

REMARKS/ARGUMENTS

Applicants thank the Examiner for the careful consideration given the present application, and respectfully request favorable reconsideration of the application in view of the comments set forth below.

Please cancel claims 2-4 and 15-31 without prejudice or disclaimer.

Claim Rejections - 35 USC §103

Claims 1, 3, 13 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bessyo (US 6,362,463) in view of JP 62-66595 (hereinafter “JP”). Applicants respectfully submit that the combination of Bessyo and JP fails to teach, suggest or otherwise render obvious every claimed feature as required to maintain the present rejection.

Specifically, amended claim 1 requires the heating apparatus to include an error signal generation circuit generating an error signal based on a difference between an input current of the AC power supply and the reference current. A frequency-modulated signal generation circuit that outputs to the dead time generation circuit a frequency-modulated signal obtained by controlling the amplitude of a rectified signal from the DC power supply based on the error signal generated by the error signal generation circuit.

The combination of Bessyo and JP fails to teach that the claimed output signal from the frequency modulated signal generation circuit is input to the dead time generation circuit. Bessyo lacks a frequency-modulated signal generation unit altogether, and the cited portions of JP fails to teach or otherwise render obvious that an output signal from the frequency conversion circuit therein, cited as the claimed frequency-modulated signal generation unit, is input to a dead time generation circuit. In fact, JP does not appear to teach a dead time generation circuit.

Further with regard to claim 1, the Office action acknowledges that the combination of Bessyo and JP lacks the claimed error signal generation circuit that generates an error signal based on a difference between an input current of the AC power supply and the reference current. Thus, the combination of Bessyo and JP fails to teach or otherwise render obvious a

frequency-modulated signal generation circuit that outputs a frequency-modulated signal based on an error signal generated by an error signal generation circuit as required by claim 1.

U.S. Patent No. 5,274,208 to Noda was cited as teaching an error signal generation circuit such as that previously claimed in claim 4, which has been canceled. But like Bessyo and JP, Applicants respectfully submit that Noda also fails to teach or otherwise render obvious that the frequency-modulated signal generation circuit outputs a frequency-modulated signal that is based on the error signal to a dead time generation circuit as required by claim 1. Further, the conduction timing determination circuit 27 cited in Noda also fails to output a frequency modulated signal obtained by controlling the amplitude of a rectified voltage/rectified current signal based on the errors signal as recited in claim 1.

For at least the above reasons, the combination of Bessyo and JP, as well as the combination of Bessyo, JP and Noda, fails to teach every limitation found in claim 1 as required to maintain a rejection of that claim under 35 U.S.C. §103(a).

The remaining claims in the present application are allowable for the limitations therein and for the limitations of the claims from which they depend.

In consideration of the foregoing analysis, it is respectfully submitted that the present application is in a condition for allowance and notice to that effect is hereby requested. If it is determined that the application is not in a condition for allowance, the examiner is invited to initiate a telephone interview with the undersigned attorney to expedite prosecution of the present application.

If there are any additional fees resulting from this communication, please charge same to our Deposit Account No. 16-0820, our Order No.: 41339.

Respectfully submitted,
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